TITANIUM OXIDE BASED THIN FILMS FOR HIGH DENSITY PASSIVE COMPONENTS INTEGRATION IN CMOS TECHNOLOGY

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***Abstract* — Investigation of titanium based thin film materials is presented in this paper as an alternative solution for the manufacturing of high density integrated resistors and capacitors in standard 0.5µm-CMOS technology. Promising thin films electrical characteristics are shown and their relation to the material properties demonstrated.**

I. Introduction

THE growing development of integrated radiofrequency and mixed signal systems stimulates the needs of high densities integrated resistors and capacitors optimized for analog applications. Values of surface densities larger than 10kΩ/sq for resistances and 10fF/µm² for capacitances are today required to improve significantly the capability of standard CMOS technology. Common titanium based thin films such as TiO_2 or TiN are both already widely used in silicon based manufacturing process. For this reason, the use of new titanium based materials can be an attractive approach to facilitate their integration as high density thin resistive and dielectric layers We choose here to investigate the electrical properties of titanium and tantalum oxide (Ti_xTa_yO) as a high-k dielectric material integrated into MOS capacitors and titanium oxynitride (TiN_xO_y) for the manufacturing of thin film resistor. Both of these materials are deposited by magnetron sputtering, which is compatible with industrial CMOS process.

Manufacturing of thin film resistors exhibiting very low (few 100Ω/sq) and very high surface resistance value (up to 1MΩ/sq) are needed respectively for radiofrequency devices and even digital systems. The potential of titanium oxynitride (TiN_xO_y) material to achieve weak dependence versus temperature has been reported in literature [1]. However, a typical density shown for TiN_xO_y Si-based resistors is limited to 2.5kΩ/sq [1]. In this study, TiN_xO_y resistive thin films were integrated in the Back End Of Line (BEOL) of 0.5µm-CMOS technology, and the effect of oxygen content in the film on the square resistance value is investigated.

The development of high-κ materials in thin film is one alternative to increase capacitance density while maintaining acceptable electrical performances. Ti_xTa_yO has been recently identified as one promising high-κ dielectric to reach the required performances [2]. We present here the extraction of intrinsic dielectric constant of $Ti_xTa_{1-x}O$ thin films from electrical characterization on MOS capacitors. The proposed extraction method allows overcoming the parasitic contribution of silicon oxide interfacial layer formed underneath the Ti_xTa_yO thin film.

II. Experimental

TiN_xO_y thin films were deposited 350°C by DC magnetron sputtering of a titanium target in reactive $Ar/N_2/O_2$ plasma, with a power density ranging from 2.5 to 4.5 W.cm ² and a deposition pressure in the $1x10^{-3}$ to $2.7x10^{3}$ mbar range. A 30 mn post deposition annealing at 450°C was performed on selected TiN_xO_y films. The integration of a 50nm thick TiN_xO_y resistive layer was performed in a 0.5µm-CMOS process.

Ti_xTa_yO thin films were deposited at 350°C on n-type silicon substrates by RF reactive sputtering of a $Ti_{0.6}Ta_{0.4}O$ target in reactive Ar/O_2 mixture, with a power density ranging from 2.5 to 4.5 W.cm-² and pressure deposition in the $9.6x10^{-4}$ to $4.5x10^{-3}$mbar range. Electrical measurements were performed on MOS capacitors, with Ti_xTa_yO thin films of thickness ranging from 25 to 320nm. The bulk chemical compositions of TiN_xO_y and Ti_xTa_yO thin films were determined by Energy Dispersive Spectroscopy (EDS) with a JEOL 5800-LV at 7kV. Electrical *I-V* characterizations on Al/ Ti_xTa_yO /Si MOS capacitors and TiN_xO_y thin film resistors were performed using an Agilent 4155C parameters analyzer for leakage measurements. *C-V* characteristics of MOS capacitors were investigated thanks to an HP4194 impedance analyzer.

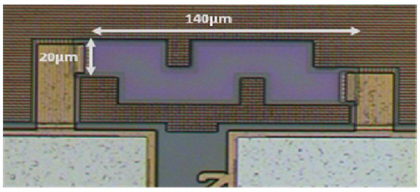

Fig.1 Optical image of a 10-square resistor integrated in the BEOL of 0.5µm CMOS technology.

III. Discussion

Fig.1 shows an optical image of a 10-square resistive TiN_xO_y thin film integrated in the Back End Of Line (BEOL) of a 0.5µm-CMOS technology. Square resistance values were deduced from the ratio of resistance value extracted from *I-V* characterization and number of squares. Deposited TiN_xO_y thin films of various chemical compositions have been integrated in CMOS. As displayed in Fig.2, the square resistance of TiN_xO_y films, deposited at 25 and 350°C, is varying versus the O/N atomic ratio checked by EDS analysis. A 30 min ex-situ annealing at 450°C under flowing oxygen leads to a further increase of the square resistance value. As the O/N ratio is increasing from 0.4 to 2.4, the square resistance is varying over five decades from 5kΩ/sq to 500MΩ/sq. The square resistance increase appears thus related to the larger oxygen content which contributes to higher bulk resistivity.

C-V and *I-V* measurements were performed on MOS $Al/Ti_xTa_yO/Si$ capacitors for Ti_xTa_yO films with thickness in the 25-320nm range deposited. In the accumulation regime of MOS capacitors, the silicon substrate acts as a bottom electrode, which allows deducing the effective permittivity of the dielectric layer. Dielectric constant was extracted for $Ti_{0.3}Ta_{0.2}O$ films with thicknesses in the 25 to 320nm range as shown in Fig.3. Strong variation of the capacitor effective dielectric constant versus the physical oxide thickness (as measured from SEM observations) is shown. The intrinsic permittivity of Ti_xTa_yO material was determined while considering the Capacitance Equivalent Thickness (CET). The slope of plot in Fig.3 allows extracting an intrinsic relative permittivity of 60 for $Ti_xTa_{1-x}O$ films with thickness ranging from 25 to 320nm. The intersection of a plot linear fit (dashed line) with the Y axis leads to an interfacial layer thickness of 3nm, which thus modifies the stacked equivalent permittivity of the structure

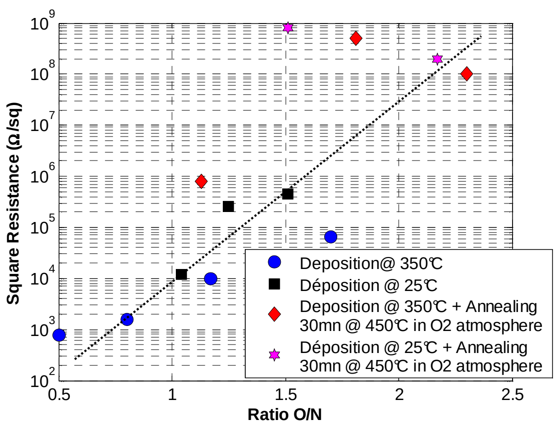

Fig.2 Variation of square resistance versus the O/N ratio in TiON thin films integrated in CMOS technology.

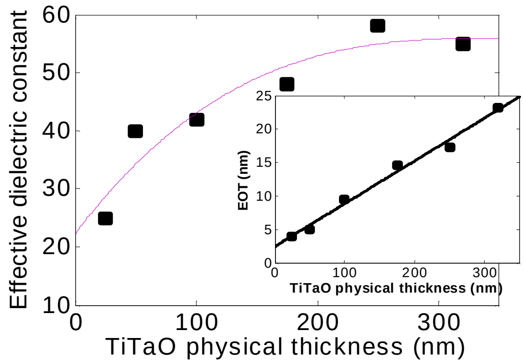

Fig.3. Effective dielectric constant and EOT of the SiO2/TiTaO stacked dielectric versus the deposited TiTaO physical thickness.

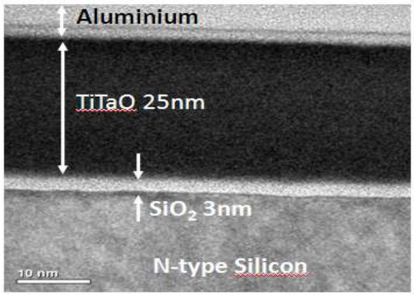

Fig.4 HRTEM image of a (Si/ $Ti_xTa_{1-x}O$ (25 nm)/Al) structure starting from the bottom interface on n-Si substrate with evidence for a 3 nm thick interfacial SiO_2 layer.

shown in Fig.3. HRTEM observations of a MOS (Al/ Ti_xTa_yO (25 nm)/Si) structure confirm the existence of a 3 nm thick interfacial dioxide layer at the bottom TiTaO/Si interface (Fig. 4).

IV. Discussion

CMOS high density Titanium based resistive and dielectric thin layers have been developed using PVD process compatible with industrial standard CMOS technology. On one hand, TiN_xO_y resistive thin films, deposited by magnetron sputtering in $Ar/O_2/N_2$ mixture have been integrated in the BEOL of a 0.5µm-CMOS technology. An accurate control of the O/N atomic ratio allows varying the square resistance value over a large scale of surface resistance values which leads to a significant improvement of the actual state of art. On the other hand, Ti_xTa_yO thin films, deposited by magnetron sputtering in Ar/O_2 plasma, were also developed for integrated capacitors. Intrinsic dielectric constant of 60 has been obtained for $Ti_{0.3}Ta_{0.2}O$ thin films with thickness ranging from 25 to 320nm.

References

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